MS51 16KB Series to MS51 32 KB Series Migration Guide

Migrating for 8-bit NuMicro® 8051 Family

Document Information

Abstract	This migration guide provides an overview of considerations for migrating from MS51 16KB series to MS51 32KB series, and includes migration considerations, the summary of the feature differences and the compatibility list of those enhanced features. Please refer to the summary of feature differences and the compatibility lists to determine the necessity of the code revision and make appropriate changes for the migration.
Apply to	NuMicro® MS51 32 KB series.

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1 Overview

This migration guide provides an overview of considerations for migrating from MS51 16KB series to MS51 32KB series. Most of the MS51 32KB series features including the core system and peripherals are fully compatible with the existing MS51 16KB series. However, in some specified cases, particularly those enhanced features, the hardware may behave differently from the existing MS51 16KB series. Table 1-1 shows summary of migration considerations; Table 1-2 shows summary of enhanced features. The subsequent chapter details the migration considerations.

Item	Description
Package	● The MS51 32KB series is fully pin-to-pin compatible with the MS51 16KB series on TSSOP20 and QFN20 packages and corresponding part number as follows: MS51FC0AE ⇋ MS51FB9AE MS51XC0BE ⇋ MS51XB9AE
Tool	● ICP Programmer Tool V3.00.6909 or later ● Nu-Link Keil Driver V3.02.6909 or later ● Nu-Link IAR Driver V3.02.6909 or later

Table 1-1 Summary of Migration Considerations

Item	Description
Peripheral	● The Flash has increased from 16 KB to 32KB ● The SRAM has increased from 1KB to 2KB ● Newly supported HXT function ● Newly supported PWM1/PWM2/PWM3 functions ● Newly supported ISO7816-3 function ● Pin interrupt channel source select condition change ● An enhanced ADC module for supporting continues conversion ● Increased ADC channels, up to 16 channels

Table 1-2 Overview of Enhanced Features in MS51 32KB Series

2 Peripheral Migration Guide

2.1 Peripheral Comparison Overview

Table 2-1 and Table 2-2 show MS51 16KB series and MS51 32KB series peripheral comparison in pin compatible packages. The differences are highlighted in BLUE.

Part Number	Flash (KB)	SRAM (KB)	ISP ROM (KB)	I/O	Timer/	PWM	Connectivity				ADC(12-Bit)	Package
							ISO-7816	UART	SPI	I²C		
MS51FBB9AE	16	1	4	18	4	6	-	2	1	1	8-ch	TSSOP20
MS51FC0AE	**32**	**2**	4	18	4	**8**	**3**	2	1	1	**10-ch**	TSSOP20

Table 2-1 MS51 16KB Series and MS51 32KB Series Peripheral Comparison in TSSOP20

Part Number	Flash (KB)	SRAM (KB)	ISP ROM (KB)	I/O	Timer/	PWM	Connectivity				ADC(12-Bit)	Package
							ISO-7816	UART	SPI	I²C		
MS51XB9BE	16	1	4	18	4	6	-	2	1	1	8-ch	QFN20
MS51XC0BE	**32**	**2**	4	18	4	**8**	**3**	2	1	1	**10-ch**	QFN20

Table 2-2 MS51 16KB Series and MS51 32KB Series Peripheral Comparison in QFN20

2.2 Peripheral Compatibility List

The differences and enhancements between the MS51 16KB series and MS51 32KB series are listed in Table 2-3.

Function	Compatibility		Description
	MS51 16KB	MS51 32KB	
APROM	16 KB	32 KB	N/A
LDROM	Begin from APROM address 3000H / 3400H / 3800H / 3C00H	Begin from APROM address 7000H / 7400H / 7800H / 7C00H	N/A
HXT	N/A	N/A	Newly supported 4~24 MHz HXT selection
ADC	N/A	ADC continues conversion	Newly supported ADC continues conversion
	N/A	N/A	Increased ADC channels, up to 16 channels
ISO7816-3	N/A	ISO7816-3	Newly supported ISO7816-3
GPIO	N/A	N/A	Pin interrupt channel source select condition change
PWM	N/A	N/A	Newly supported PWM1/PWM2/PWM3

Table 2-3 MS51 16KB Series and MS51 32KB Series Comparison

Table 2-4 lists the pin compatible packages between MS51 16KB series and MS51 32KB series

MS51 16KB Series	MS51 32KB Series	Package
MS51XB9AE		QFN 20*
MS51XB9BE	MS51XC0BE	QFN 20*
MS51FB9AE	MS51FC0AE	TSSOP20
	MS51EC0AE	TSSOP28
	MS51PC0AE	LQFP32
	MS51TC0AE	QFN33
Note:* QFN20 package with two kinds of different dimensions.		

Table 2-4 MS51 16KB Series and MS51 32KB Series Pin Compatible Packages

3 Hardware Migration Guide

3.1 Multi-Function Pin Comparison

The MS51 32KB series is fully pin-to-pin compatible with the MS51 16KB series in TSSOP20 and QFN20 packages, the product can be easily upgraded by replacing the chip. Table 3-1 and Table 3-2 show the differences in multi-function pin for TSSOP20 and QFN20 respectively.

3.1.1 TSSOP20 Differences

Pin Number	MS51FB9AE	MS51FC0AE	Multi-Function Description
1	P0.5		Port 0 bit 5
	PWM0_CH2		PWM0 output channel 2
	IC6		Input capture channel 6
	T0		External count input to Timer/Counter 0 or its toggle output.
	ADC_CH4		ADC input channel 4
	-	PWM2_CH0	PWM2 output channel 0
	-	UART3_TXD	Serial port 3 transmit data output.
2	P0.6		Port 0 bit 6
	UART0_TXD		Serial port 0 transmit data output.
	ADC_CH3		ADC input channel 3
3	P0.7		Port 0 bit 7
	UART0_RXD		Serial port 0 receive input
	ADC_CH2		ADC input channel 2
4	P2.0		Port 2 bit 0 input pin available when RPD (CONFIG0.2) is programmed as 0
	nRESET		nRESET pin is a Schmitt trigger input pin for hardware device reset. A low on this pin resets the device. nRESETpin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND. **Note:** It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.
5	P3.0		Port 3 bit 0
	INT0		External interrupt 0 input
	OSCIN		If the ECLK mode is enabled, Xin is the external clock input pin
	ADC_CH1		ADC input channel 1
	-	UART2_TXD	Serial port 2 transmit data output.
	-	SPI0_MOSI	SPI0 master output/slave input
6	P1.7		Port 1 bit 7
	INT1		External interrupt 1 input

Pin Number	MS51FB9AE	MS51FC0AE	Multi-Function Description
	ADC_CH0		ADC input channel 0
	-	UART2_RXD	Serial port 2 receive input
	-	SPI0_CLK	SPI0 clock
7	VSS		GROUND
8	P1.6		Port 1 bit 6
	ICE_DAT		ICP / OCD data input or output. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.
	UART1_TXD		Serial port 1 transmit data output
	I2C0_SDA		I^2C0 data
9	VDD		Supply voltage V_{DD} for operation.
10	P1.5		Port 1 bit 5
	PWM0_CH5		PWM0 output channel 5
	IC7		Input capture channel 7
	SPI0_SS		SPI0 slave select input.
	-	UART3_RXD	Serial port 3 receive input
	-	PWM3_CH1	PWM3 output channel 1
11	P1.4		Port 1 bit 4
	PWM0_CH1		PWM0 output channel 1
	I2C0_SDA		I^2C0 data
	PWM0_BRAKE		PWM0 Fault Brake input
	-	ADC_CH14	ADC input channel 14
	-	PWM1_CH1	PWM1 output channel 1
12	P1.3		Port 1 bit 3
	I2C0_SCL		I^2C0 clock
	STADC		External start ADC trigger
	-	ADC_CH13	ADC input channel 13
13	P1.2		Port 1 bit 2
	PWM0_CH0		PWM0 output channel 0
	IC0		Input capture channel 0
	-	UART3_TXD	Serial port 3 transmit data output
	-	PWM1_CH0	PWM1 output channel 0
14	P1.1		Port 1 bit 1
	PWM0_CH1		PWM0 output channel 1

Pin Number	MS51FB9AE	MS51FC0AE	Multi-Function Description
	IC1		Input capture channel 1
	ADC_CH7		ADC input channel 7
	CLKO		System clock output
	-	UART3_RXD	Serial port 3 receive input
	-	PWM1_CH1	PWM1 output channel 1
15	P1.0		Port 1 bit 0
	PWM0_CH2		PWM0 output channel 2
	IC2		Input capture channel 2
	SPI0_CLK		SPI0 clock
	-	UART1_TXD	Serial port 1 transmit data output
	-	PWM2_CH0	PWM2 output channel 0
16	P0.0		Port 0 bit 0
	PWM0_CH3		PWM0 output channel 3
	SPI0_MOSI		SPI0 master output/slave input
	IC3		Input capture channel 3
	T1		External count input to Timer/Counter 1 or its toggle output
	-	UART1_RXD	Serial port 1 receive input
	-	HXTIN	External 4~24 MHz (high speed) crystal input pin.
	-	PWM2_CH1	PWM2 output channel 1
17	P0.1		Port 0 bit 1
	PWM0_CH4		PWM0 output channel 4
	IC4		Input capture channel 4
	SPI0_MISO		SPI0 master input/slave output.
	-	HXTOUT	External 4~24 MHz (high speed) crystal output pin.
	-	PWM3_CH0	PWM3 output channel 0
18	P0.2		Port 0 bit 2
	ICE_CLK		ICE / ICP clock input. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin.
	UART1_RXD		Serial port 1 receive input
	I2C0_SCL		I^2C0 clock
19	P0.3		Port 0 bit 3
	PWM0_CH5		PWM0 output channel 5
	IC5		Input capture channel 5

Pin Number	MS51FB9AE	MS51FC0AE	Multi-Function Description
	ADC_CH6		ADC input channel 6
	-	UART2_TXD	Serial port 2 transmit data output
	-	PWM3_CH1	PWM3 output channel 1
20	P0.4		Port 0 bit 4
	PWM0_CH3		PWM0 output channel 3
	IC3		Input capture channel 3
	ADC_CH5		ADC input channel 5
	STADC		External start ADC trigger
	-	UART2_RXD	Serial port 2 receive input
	-	PWM2_CH1	PWM2 output channel 1

Table 3-1 The Differences in Multi-Function Pin for TSSOP20 Package

3.1.2 QFN20 Differences

Pin Number	MS51XB9AE	MS51XB9BE	MS51XC0BE	Multi-Function Description
1	P0.7	-	-	Port 0 bit 7
	ADC_CH2	-	-	ADC input channel 2
	UART0_RXD	-	-	Serial port 0 receive input
	-	P2.0	P2.0	Port 2 bit 0
	-	nRESET	nRESET	nRESET pin is a Schmitt trigger input pin for hardware device reset. A low on this pin resets the device. nRESETpin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND. **Note:** It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.
2	P1.7	-	-	Port 1 bit 7
	ADC_CH0	-	-	ADC input channel 0
	INT1	-	-	External interrupt 1 input
	-	P3.0	P3.0	Port 3 bit 0
	-	ADC_CH1	ADC_CH1	ADC input channel 1
	-	OSCIN	OSCIN	If the EXTEN[1:0] = 11b, OSCIN is the external clock input pin.
	-	INT0	INT0	External interrupt 0 input
	-	-	UART2_TXD	Serial port 2 transmit data output
	-	-	SPI0_MOSI	SPI0 master output/slave input

Pin Number	MS51XB9AE	MS51XB9BE	MS51XC0BE	Multi-Function Description
	-	-	PWM2_CH1	PWM2 output channel 1
3	VSS	-	-	GROUND
	-	P1.7	P1.7	Port 1 bit 7
	-	ADC_CH0	ADC_CH0	ADC input channel 0
	-	INT1	INT1	External interrupt 1 input
	-	-	UART2_RXD	Serial port 2 receive input
	-	-	SPI0_CLK	SPI0 clock
	-	-	PWM3_CH0	PWM3 output channel 0
4	P1.6	-	-	Port 1 bit 6
	ICE_DAT	-	-	ICP / OCD data input or output. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.
	UART1_TXD	-	-	Serial port 1 transmit data output
	I2C0_SDA	-	-	I^2C0 data
	-	VSS	VSS	GROUND
5	VDD	-	-	Supply voltage V_{DD} for operation.
	-	P1.6	P1.6	Port 1 bit 6
	-	ICE_DAT	ICE_DAT	ICP / OCD data input or output. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.
	-	UART1_TXD	UART1_TXD	Serial port 1 transmit data output
	-	I2C0_SDA	I2C0_SDA	I^2C0 data
6	P1.5	-	-	Port 1 bit 5
	PWM0_CH5	-	-	PWM0 output channel 5
	IC7	-	-	Input capture channel 7
	SPI0_SS	-	-	SPI0 slave select input
	-	VDD	VDD	Supply voltage V_{DD} for operation.
7	P1.0	-	-	Port 1 bit 0
	PWM0_CH2	-	-	PWM0 output channel 2
	IC2	-	-	Input capture channel 2
	SPI0_CLK	-	-	SPI0 clock
	-	P1.5	P1.5	Port 1 bit 5
	-	PWM0_CH5	PWM0_CH5	PWM0 output channel 5
	-	IC7	IC7	Input capture channel 7

Pin Number	MS51XB9AE	MS51XB9BE	MS51XC0BE	Multi-Function Description
	-	SPI0_SS	SPI0_SS	SPI0 slave select input
	-	-	UART3_TXD	Serial port 3 transmit data output
	-	-	PWM3_CH1	PWM3 output channel 1
8	P1.1	-	-	Port 1 bit 1
	PWM0_CH1	-	-	PWM0 output channel 1
	IC1	-	-	Input capture channel 1
	ADC_CH7	-	-	ADC input channel 7
	CLKO	-	-	System clock output
	-	P1.4	P1.4	Port 1 bit 4
	-	PWM0_CH1	PWM0_CH1	PWM0 output channel 1
	-	I2C0_SDA	I2C0_SDA	I^2C0 data
	-	PWM0_BRAKE	PWM0_BRAKE	PWM0 Fault Brake input
	-	-	ADC_CH14	ADC input channel 14
	-	-	PWM1_CH1	PWM1 output channel 1
9	P1.2	-	-	Port 1 bit 2
	PWM0_CH0	-	-	PWM0 output channel 0
	IC0	-	-	Input capture channel 0
	-	P1.3	P1.3	Port 1 bit 3
	-	I2C0_SCL	I2C0_SCL	I^2C0 clock
	-	STADC	STADC	External start ADC trigger
	-	-	ADC_CH13	ADC input channel 13
10	P1.4	-	-	Port 1 bit 4
	PWM0_CH1	-	-	PWM0 output channel 1
	I2C0_SDA	-	-	I^2C0 data
	PWM0_BRAKE	-	-	PWM0 Fault Brake input
	-	P1.2	P1.2	Port 1 bit 2
	-	PWM0_CH0	PWM0_CH0	PWM0 output channel 0
	-	IC0	IC0	Input capture channel 0
	-	-	UART3_TXD	Serial port 3 transmit data output
	-	-	PWM1_CH0	PWM1 output channel 0
11	P1.3	-	-	Port 1 bit 3
	I2C0_SCL	-	-	I^2C0 clock

Pin Number	MS51XB9AE	MS51XB9BE	MS51XC0BE	Multi-Function Description
	STADC	-	-	External start ADC trigger
	-	P1.1	P1.1	Port 1 bit 1
	-	ADC_CH7	ADC_CH7	ADC input channel 7
	-	CLKO	CLKO	System clock output
	-	IC1	IC1	Input capture channel 1
	-	PWM0_CH1	PWM0_CH1	PWM0 output channel 1
	-	-	UART3_RXD	Serial port 3 receive input
	-	-	PWM1_CH1	PWM1 output channel 1
12	P0.0	-	-	Port 0 bit 0
	PWM0_CH3	-	-	PWM0 output channel 3
	SPI0_MOSI	-	-	SPI0 master output/slave input
	IC3	-	-	Input capture channel 3
	T1	-	-	External count input to Timer/Counter 1 or its toggle output
	-	P1.0	P1.0	Port 1 bit 0
	-	PWM0_CH2	PWM0_CH2	PWM0 output channel 2
	-	IC2	IC2	Input capture channel 2
	-	SPI0_CLK	SPI0_CLK	SPI0 clock
	-	-	UART1_TXD	Serial port 1 transmit data output
	-	-	PWM2_CH0	PWM2 output channel 0
13	P0.1	-	-	Port 0 bit 1
	PWM0_CH4	-	-	PWM0 output channel 4
	IC4	-	-	Input capture channel 4
	SPI0_MISO	-	-	SPI0 master input/slave output.
	-	P0.0	P0.0	Port 0 bit 0
	-	PWM0_CH3	PWM0_CH3	PWM0 output channel 3
	-	SPI0_MOSI	SPI0_MOSI	SPI0 master output/slave input
	-	IC3	IC3	Input capture channel 3
	-	T1	T1	External count input to Timer/Counter 1 or its toggle output
	-	-	UART1_RXD	Serial port 1 receive input
	-	-	HXTIN	External 4~24 MHz (high speed) crystal input pin.
	-	-	PWM2_CH1	PWM2 output channel 1
14	P0.2	-	-	Port 0 bit 2

Pin Number	MS51XB9AE	MS51XB9BE	MS51XC0BE	Multi-Function Description
	ICE_CLK	-	-	ICE / ICP clock input. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin.
	UART1_RXD	-	-	Serial port 1 receive input
	I2C0_SCL	-	-	I^2C0 clock
	-	P0.1	P0.1	Port 0 bit 1
	-	PWM0_CH4	PWM0_CH4	PWM0 output channel 4
	-	IC4	IC4	Input capture channel 4
	-	SPI0_MISO	SPI0_MISO	SPI0 master input/slave output.
	-	-	HXTOUT	External 4~24 MHz (high speed) crystal output pin
	-	-	PWM3_CH0	PWM3 output channel 0
15	P0.3	-	-	Port 0 bit 3
	PWM0_CH5	-	-	PWM0 output channel 5
	IC5	-	-	Input capture channel 5
	ADC_CH6	-	-	ADC input channel 6
	-	P0.2	P0.2	Port 0 bit 2
	-	ICE_CLK	ICE_CLK	ICE / ICP clock input. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin.
	-	UART1_RXD	UART1_RXD	Serial port 1 receive input
	-	I2C0_SCL	I2C_SCL	I^2C0 clock
16	P0.4	-	-	Port 0 bit 4
	IC3	-	-	Input capture channel 3
	PWM0_CH3	-	-	PWM0 output channel 3
	STADC	-	-	External start ADC trigger
	ADC_CH5	-	-	ADC input channel 5
	-	P0.3	P0.3	Port 0 bit 3
	-	PWM0_CH5	PWM0_CH5	PWM0 output channel 5
	-	IC5	IC5	Input capture channel 5
	-	ADC_CH6	ADC_CH6	ADC input channel 6
	-	-	UART2_TXD	Serial port 2 transmit data output
	-	-	PWM3_CH1	PWM3 output channel 1
17	P3.0	-	-	Port 3 bit 0
	INT0	-	-	External interrupt 0 input

Pin Number	MS51XB9AE	MS51XB9BE	MS51XC0BE	Multi-Function Description
	OSCIN	-	-	If the EXTEN[1:0] = 11b, OSCIN is the external clock input pin.
	ADC_CH1	-	-	ADC input channel 1
	-	P0.4	P0.4	Port 0 bit 4
	-	PWM0_CH3	PWM0_CH3	PWM0 output channel 3
	-	IC3	IC4	Input capture channel 4
	-	ADC_CH5	ADC_CH5	ADC input channel 5
	-	STADC	STADC	External start ADC trigger
	-	-	UART2_RXD	Serial port 2 receive input
	-	-	PWM2_CH1	PWM2 output channel 1
18	P2.0	-	-	Port 2 bit 0 input pin available when RPD (CONFIG0.2) is programmed as 0
	nRESET	-	-	nRESET pin is a Schmitt trigger input pin for hardware device reset. A low on this pin resets the device. nRESETpin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND. **Note:** It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.
	-	P0.5	P0.5	Port 0 bit 5
	-	PWM0_CH2	PWM0_CH2	PWM0 output channel 2
	-	IC6	IC6	Input capture channel 6
	-	T0	T0	External count input to Timer/Counter 0 or its toggle output
	-	ADC_CH4	ADC_CH4	ADC input channel 4
	-	-	PWM2_CH0	PWM2 output channel 0
	-	-	UART3_TXD	Serial port 3 transmit data output
19	P0.6	P0.6	P0.6	Port 0 bit 6
	ADC_CH3	ADC_CH3	ADC_CH3	ADC input channel 3
	UART0_TXD	UART0_TXD	UART0_TXD	Serial port 0 transmit data output
20	P0.5	-	-	Port 0 bit 5
	PWM0_CH2	-	-	PWM0 output channel 2
	IC6	-	-	Input capture channel 6
	T0	-	-	External count input to Timer/Counter 0 or its toggle output
	ADC_CH4	-	-	ADC input channel 4
	-	P0.7	P0.7	Port 0 bit 7
	-	UART0_RXD	UART0_RXD	Serial port 0 receive input
	-	ADC_CH2	ADC_CH2	ADC input channel 2

Table 3-2 The Differences in Multi-Function Pin for QFN20 Package

3.2 External Clock Pin

The MS51 32KB series support a new feature, 4 MHz to 24 MHz high-speed crystal(HXT). When HXT is used as the system clock, X_{IN} and X_{OUT} are the input and output, respectively. Figure 3-2 and Figure 3-2 show MS51 16KB series and MS51 32KB series clock system block diagram, respectively.

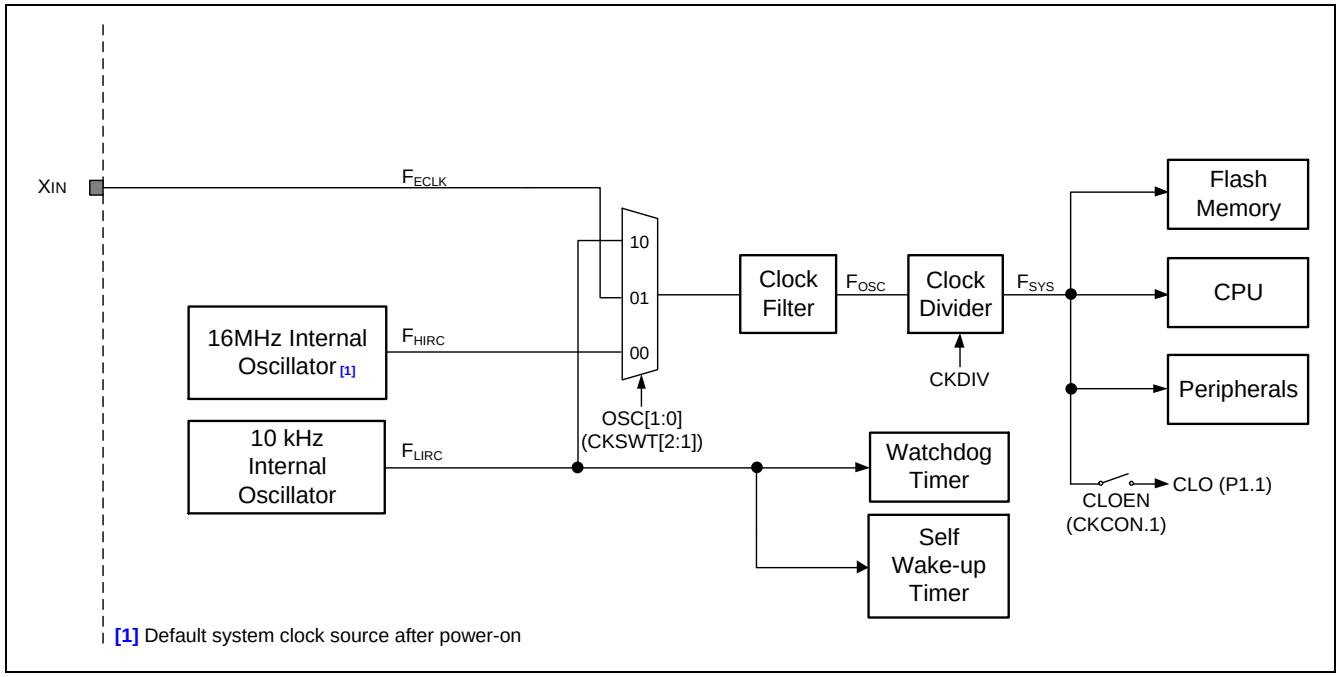

Figure 3-1 Series Clock System Block Diagram for MS51 16KB

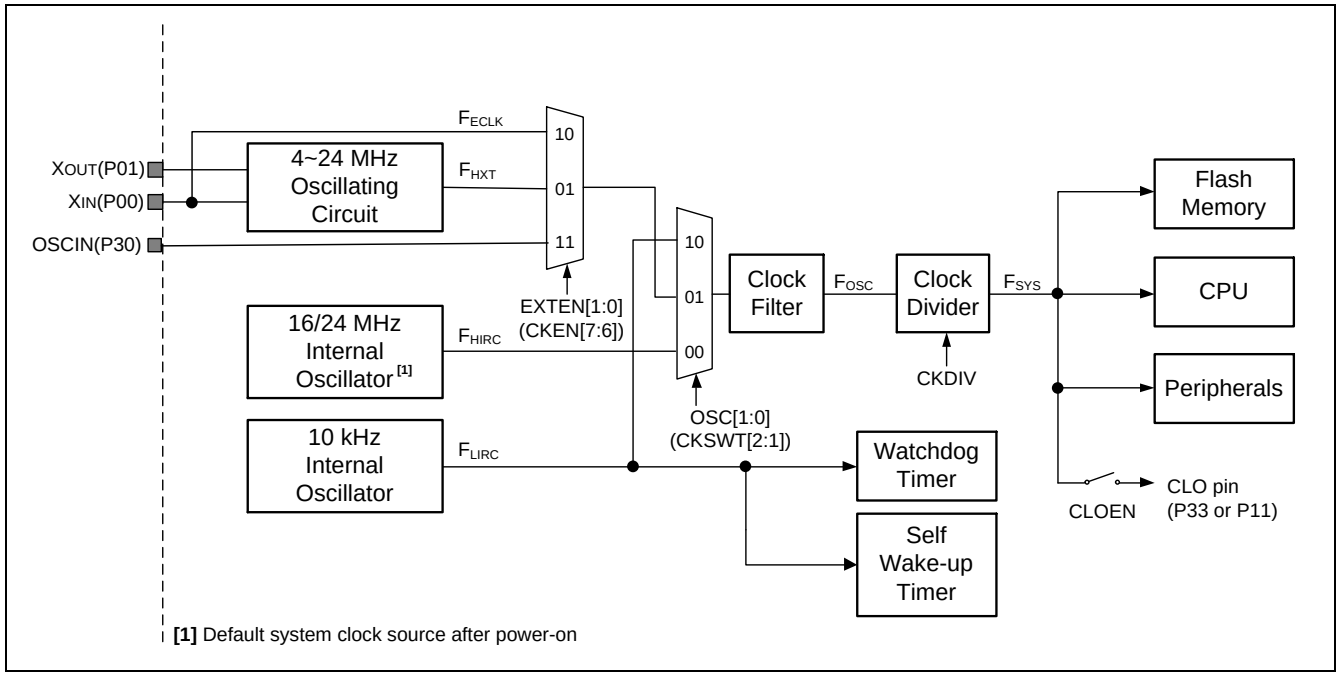

Figure 3-2 Clock System Block Diagram for MS51 32KB

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4.1 Clock System

4.1.1 HXT Selection

MS51 32 KB series support a new feature, 4 MHz to 24 MHz high-speed crystal(HXT). Because of this, the EXTEN[1:0](CKSWT[7:6]) register has been extended to 3 options instead of 1.

4.1.1.1 Register

The MS51 32KB series extends option of EXTEN[1:0](CKSWT [7:6]) register, which can be used to select HXT as input source. The register details are as follows:

- The new features are highlighted in BLUE and bits marked in "-" are reserved.
- "All register pages" means that the register can access on page 0 and page 1.
- "Timed Access(TA)" means that the TA protected SFR have a timed write enable window. A writing permission window is opened for 4 clock cycles during this period that user may write to protected SFR. Otherwise, the write will be discarded. The suggested code for opening the timed access window is shown below.

Register	SFR Address	Reset Value
CKEN	97H, All register pages, TA protected	0011_0000b

7	6	5	4	3	2	1	0
EXTEN[1:0]		HIRCEN	-	-	-	-	CKSWTF
R/W		R/W	-	-	-	-	R

Bit	Name	Description
[7:6]	EXTEN[1:0]	**External clock source enable** 11 = External clock input via XIN Enabled. Others = external clock input is disable. P30 work as general purpose I/O.

Table 4-1 Clock Enable for MS51 16KB Series

Register	SFR Address	Reset Value
CKEN	97H, **Page 0**, TA protected	0011_0000b

7	6	5	4	3	2	1	0
EXTEN[1:0]		HIRCEN	LIRCEN	-	-	-	CKSWTF
R/W		R/W	R/W	-	-	-	R

Bit	Name	Description
[7:6]	EXTEN[1:0]	**External clock source enable** 11 = External clock input via OSCIN (P30) Enabled **10 = External clock input via HXTIN (P00) Enabled** **01 = External crystal 4~24 MHz Enabled** 00 = external clock input is disable. P30/P00/P01 work as general purpose I/O or other functions.

Table 4-2 Clock Enable for MS51 32KB Series

4.2 Interrupt System

4.2.1 Interrupt Vectors

The interrupt source has increased from 18 on the MS51 16KB series to 32 on the MS51 32KB series. The additional interrupt sources are listed in Table 4-3 and highlighted in BLUE.

Source	Vector Addess	Vector Number	Source	Vector Address	Vector Number
Reset	0000H	-	Input capture interrupt	0063H	12
External interrupt 0	0003H	0	PWM0 interrupt	006BH	13
Timer 0 overflow	000BH	1	Fault Brake interrupt	0073H	14
External interrupt 1	0013H	2	Serial port 1 interrupt	007BH	15
Timer 1 overflow	001BH	3	Timer 3 overflow	0083H	16
Serial port 0 interrupt	0023H	4	Self Wake-up Timer interrupt	008BH	17
Timer 2 event	002BH	5	**PWM1 interrupt**	**0093H**	**18**
I^2C status/timer-out interrupt	0033H	6	**PWM2 interrupt**	**009BH**	**19**
Pin interrupt	003BH	7	**PWM3 interrupt**	**00A3H**	**20**
Brown-out detection interrupt	0043H	8	**SC0 interrupt**	**00ABH**	**21**
SPI interrupt	004BH	9	**SC1 interrupt**	**00B3H**	**22**
WDT interrupt	0053H	10	**SC2 interrupt**	**00BBH**	**23**
ADC interrupt	005BH	11	-	-	-

Table 4-3 Interrupt Vectors for MS51 32KB series

4.3 GPIO

4.3.1 Pin Interrupt Source Selection

Figure 4-1 and Figure 4-2 show pin interface block diagram in MS51 16KB series and MS51 32KB series, respectively. Take pin interrupt channel 0 as example, only P0.0, P1.0, P2.0 and P3.0 can trigger the PIF0 interrupt from any of these inputs in MS51 16KB series, but MS51 32KB series can trigger the PIF0 interrupt by any I/O pin.

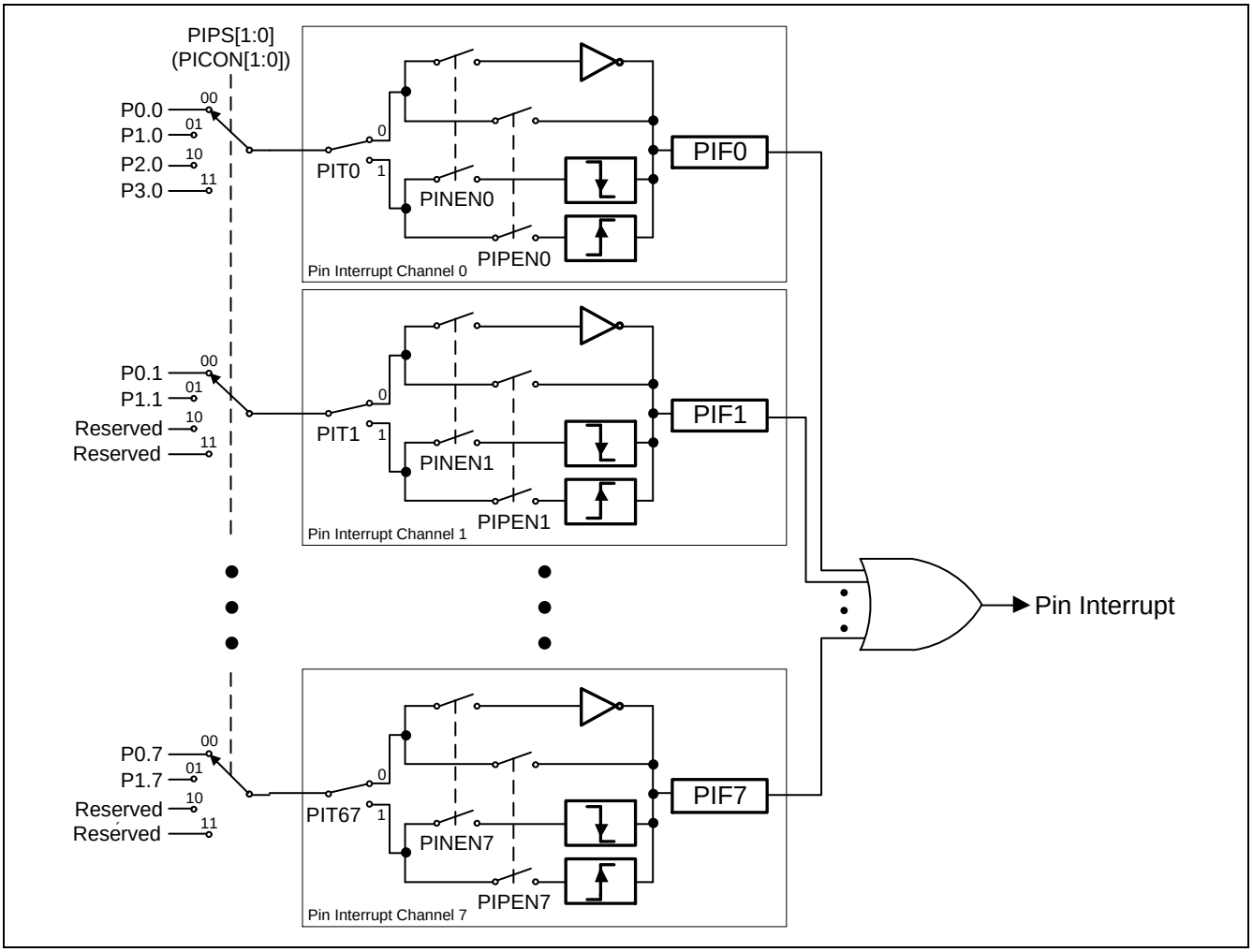

Figure 4-1 Pin Interface Block Diagram for MS51 16KB Series

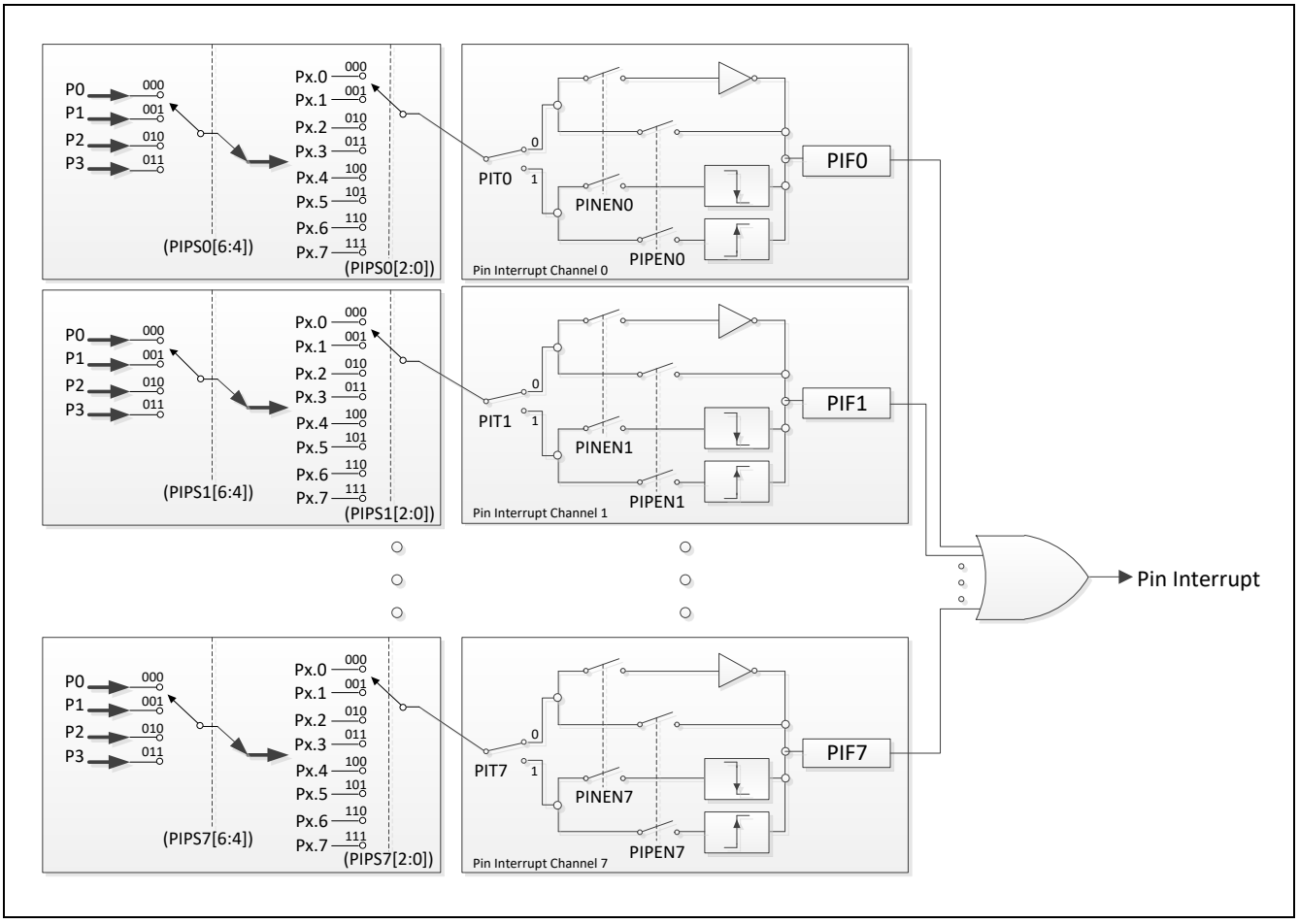

Figure 4-2 Pin Interface Block Diagram for MS51 32KB series

4.3.1.1 Register

The register details are as follows:

- The new features are highlighted in BLUE and bits marked in "-" are reserved.
- "All register pages" means that the register can access on page 0 and page 1.

Register	SFR Address	Reset Value
PICON	E9H, All register pages	0000_0000 b

7	6	5	4	3	2	1	0
PIT67	PIT45	PIT3	PIT2	PIT1	PIT0	PIPS[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Bit	Name	Description
[7]	PIT67	**Pin interrupt channel 6 and 7 type select** This bit selects which type that pin interrupt channel 6 and 7 is triggered. 0 = Level triggered. 1 = Edge triggered.
[6]	PIT45	**Pin interrupt channel 4 and 5 type select** This bit selects which type that pin interrupt channel 4 and 5 is triggered. 0 = Level triggered. 1 = Edge triggered.
[5]	PIT3	**Pin interrupt channel 3 type select** This bit selects which type that pin interrupt channel 3 is triggered. 0 = Level triggered. 1 = Edge triggered
[4]	PIT2	**Pin interrupt channel 2 type select** This bit selects which type that pin interrupt channel 2 is triggered. 0 = Level triggered. 1 = Edge triggered.
[3]	PIT1	**Pin interrupt channel 1 type select** This bit selects which type that pin interrupt channel 1 is triggered. 0 = Level triggered. 1 = Edge triggered.
[2]	PIT0	**Pin interrupt channel 0 type select** This bit selects which type that pin interrupt channel 0 is triggered. 0 = Level triggered. 1 = Edge triggered.
[1:0]	PIPS[:0]	**Pin interrupt port select** This field selects which port is active as the 8-channel of pin interrupt. 00 = Port 0. 01 = Port 1. 10 = Port 2. 11 = Port 3.

Table 4-4 Pin Interrupt Control for MS51 16KB Series

Register	SFR Address	Reset Value
PINEN	EAH, All register pages	0000_0000b

7	6	5	4	3	2	1	0
PINEN7	PINEN6	PINEN5	PINEN4	PINEN3	PINEN2	PINEN1	PINEN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 4-5 Pin Interrupt Negative Polarity Enable for MS51 16KB Series

Register	SFR Address	Reset Value
PIPEN	EBH, All register pages	0000_0000b

7	6	5	4	3	2	1	0
PIPEN7	PIPEN6	PIPEN5	PIPEN4	PIPEN3	PIPEN2	PIPEN1	PIPEN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 4-6 Pin Interrupt Positive Polarity Enable for MS51 16KB Series

Register	SFR Address	Reset Value
PIF	ECH, All register pages	0000_0000b

7	6	5	4	3	2	1	0
PIF7	PIF6	PIF5	PIF4	PIF3	PIF2	PIF1	PIF0
R (level) R/W (edge)	R (level) R/W (edge)	R (level) R/W (edge)	R (level) R/W (edge)	R (level) R/W (edge)	R (level) R/W (edge)	R (level) R/W (edge)	R (level) R/W (edge)

Table 4-7 Pin Interrupt Flags for MS51 16KB Series

Register	SFR Address	Reset Value
PICON	E9H, **Page 0**	**0011 _0100 b**

7	6	5	4	3	2	1	0
PIT7	**PIT6**	**PIT5**	**PIT4**	**PIT3**	**PIT2**	**PIT1**	**PIT0**
R/W	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**

Bit	Name	Description
[7]	PIT7	**Pin interrupt channel 7 type select** This bit selects which type that pin interrupt channel 7 is triggered.

		0 = Level triggered. 1 = Edge triggered.
[6]	PIT6	**Pin interrupt channel 6 type select** This bit selects which type that pin interrupt channel 6 is triggered. 0 = Level triggered. 1 = Edge triggered.
[5]	PIT5	**Pin interrupt channel 5 type select** This bit selects which type that pin interrupt channel 5 is triggered. 0 = Level triggered. 1 = Edge triggered.
[4]	PIT4	**Pin interrupt channel 4 type select** This bit selects which type that pin interrupt channel 4 is triggered. 0 = Level triggered. 1 = Edge triggered.
[3]	PIT3	**Pin interrupt channel 3 type select** This bit selects which type that pin interrupt channel 3 is triggered. 0 = Level triggered. 1 = Edge triggered.
[2]	PIT2	**Pin interrupt channel 2 type select** This bit selects which type that pin interrupt channel 2 is triggered. 0 = Level triggered. 1 = Edge triggered.
[1:0]	PIT1	**Pin interrupt channel 1 type select** This bit selects which type that pin interrupt channel 1 is triggered. 0 = Level triggered. 1 = Edge triggered.

Table 4-8 Pin Interrupt Control for MS51 32KB Series

Register	SFR Address	Reset Value
PINEN	EAH, **Page 0**	0000_0000b

7	6	5	4	3	2	1	0
PINEN7	PINEN6	PINEN5	PINEN4	PINEN3	PINEN2	PINEN1	PINEN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 4-9 Pin Interrupt Negative Polarity Enable for MS51 32KB Series

Register	SFR Address	Reset Value
PIPEN	EBH, **Page 0**	0000_0000b

7	6	5	4	3	2	1	0
PIPEN7	PIPEN6	PIPEN5	PIPEN4	PIPEN3	PIPEN2	PIPEN1	PIPEN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 4-10 Pin Interrupt Positive Polarity Enable for MS51 32KB Series

Register	SFR Address	Reset Value
PIF	ECH, **Page 0**	0000_0000b

7	6	5	4	3	2	1	0
PIF7	PIF6	PIF5	PIF4	PIF3	PIF2	PIF1	PIF0
R (level) R/W (edge)	R (level) R/W (edge)	R (level) R/W (edge)	R (level) R/W (edge)	R (level) R/W (edge)	R (level) R/W (edge)	R (level) R/W (edge)	R (level) R/W (edge)

Table 4-11 Pin Interrupt Flags for MS51 32KB Series

Register	SFR Address	Reset Value
PIPS7	F7H, page 2	0000_0000 b
PIPS6	FFH, page 2	0000_0000 b
PIPS5	FEH, page 2	0000_0000 b
PIPS4	FDH, page 2	0000_0000 b
PIPS3	FCH, page 2	0000_0000 b
PIPS2	FBH, page 2	0000_0000 b
PIPS1	FAH, page 2	0000_0000 b
PIPS0	F9H, page 2	0000_0000 b

7	6	5	4	3	2	1	0
-	PSEL[2:0]			-	BSEL[2:0]		

-	R/W	-	R/W

Bit	Name	Description
[6:4]	PSEL[2:0]	**Pin interrupt channel Port select** 000 = P0 PORT. 001 = P1 PORT. 010 = P2 PORT. 011 = P3 PORT. 100 = Reserved. 101 = Reserved. 110 = Reserved. 111 = Reserved.
[2:0]	BSEL[2:0]	**Pin interrupt channel bit select** 000 = Pn.0. 001 = Pn.1 010 =.Pn.2 011 = Pn.3. 100 = Pn.4. 101 = Pn.5. 110 = Pn.6. 111 = Pn.7. n is the PORT number, which is selected by PSEL[2:0].

Table 4-12 Pin Interrupt Control for MS51 32KB Series

4.4 PWM

4.4.1 PWM1/2/3

The PWM module has increased from 1 on the MS51 16KB series to 4 on the MS51 32KB series. The key features and limitation provided by the PWM1/2/3 module are listed below:

- Support individual configurable period and duty
- Each of two PWM1/2/3 can be configured as one of independent mode, complementary mode, or synchronous mode
- All PWM group can start at the same time
- Fault Brake function are only valid in PWM0

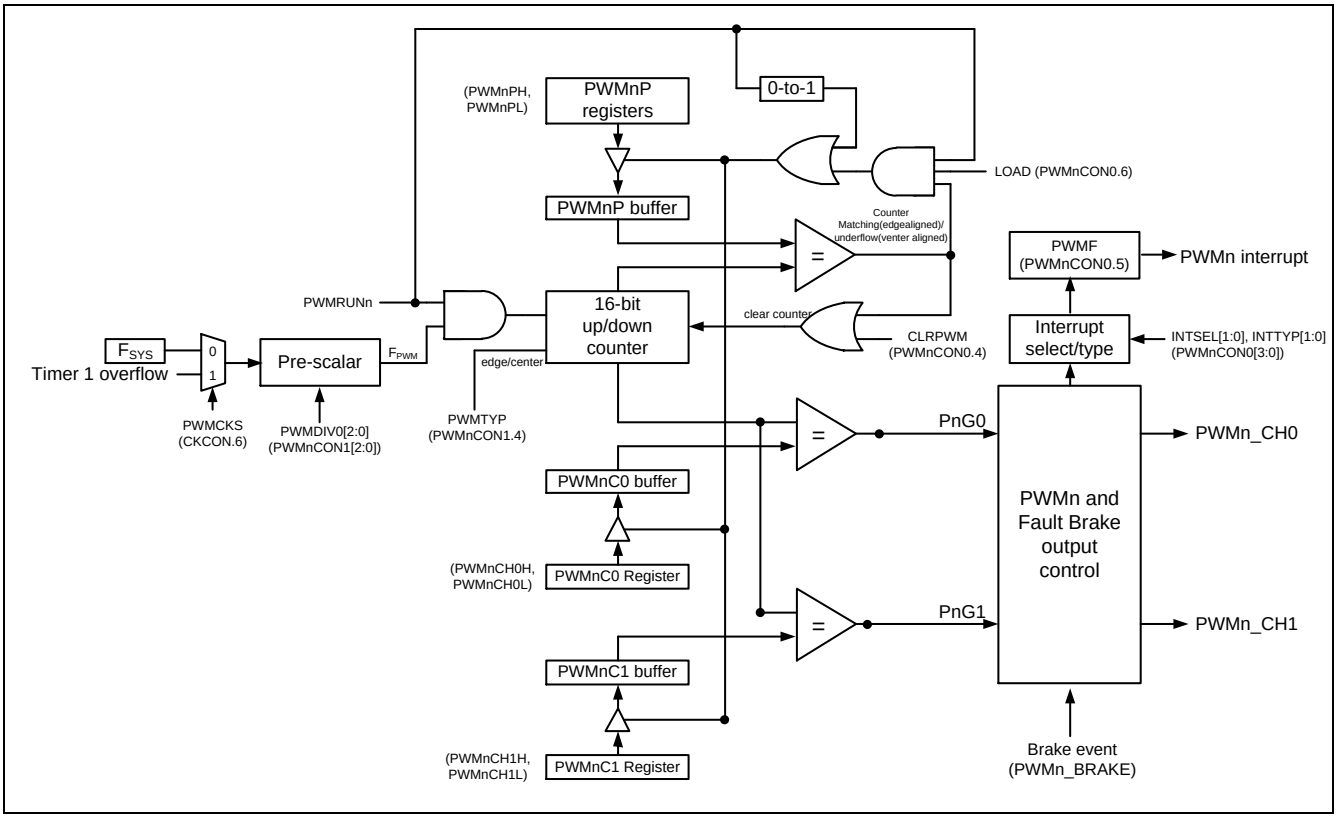

Figure 4-3 PWM1/2/3 Block Diagram for MS51 32KB Series

4.5 ISO 7816-3

4.5.1 SC0~2 & UART2 ~ 4

The MS51 32KB series includes a feature, ISO 7816-3 interface controller. This controller also provides UART emulation for high precision baud rate communication. The key features provided by the ISO 7816-3 interface controller are listed below:

- ISO-7816-3 T = 0, T = 1 compliant
- Programmable transmission clock frequency
- Programmable extra guard time selection
- Supports auto inverse convention function

4.6 ADC

The main differences between the MS51 16KB series and the MS51 32KB series are:

- The MS51 32KB series which increase ADC channels, up to 16 channels.
- The MS51 32KB series includes a new feature, ADC continues conversion. See section 4.6.2 for more details.

4.6.1 ADC Channels

The MS51 32KB series which increase ADC channels, up to 16 channels.

4.6.1.1 Register

The MS51 32KB series has two new registers, ADCAQT1[2:0](ADCCON3[3:1]) and AINDIDS1. ADCAQT1[2:0](ADCCON3[3:1]) can be used to configure the acquisition time for ADC channel 9~15 sampling. AINDIDS1 can be used to disable ADC channel digital input path. The register details are as follows:

Register	SFR Address	Reset Value
ADCCON3	86H, Page 2	0000_0000 b

7	6	5	4	3	2	1	0
-	-	HIE	CONT	ADCAQT1[2:0]			CKSWTF
-	-	R/W	R/W	R/W			R

Bit	Name	Description
[3:1]	ADCAQT1	**ADC acquisition time 1** This 3-bit field decides the acquisition time for ADC AIN9~AIN15 sampling, following by equation below: ADC acquisition time = $\frac{4 * ADCAQT + 6}{F_{ADC}}$. The default and minimum acquisition time is 6 ADC clock cycles. Note that this field should not be changed when ADC is in converting.

Table 4-13 ADC Control Register 3 for MS51 32KB Series

Register	SFR Address	Reset Value
AINDIDS1	99H, Page 2	0000_0000 b

7	6	5	4	3	2	1	0
P25DIDS	P14DIDS	P13DIDS	P24DIDS	P23DIDS	P22DIDS	P21DIDS	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	-

Bit	Name	Description
n	PnnDIDS	**ADC Channel digital input disable** 0 = ADC channel n digital input Enabled. 1 = ADC channel n digital input Disabled. ADC channel n is read always 0.

Table 4-14 ADC Channel Digital Input Disconnect for MS51 32KB Series

4.6.2 ADC Continues Conversion

The MS51 32KB series includes a new feature, ADC continues conversion, which auto store the 12-bit A/D conversion result into XRAM buffer.

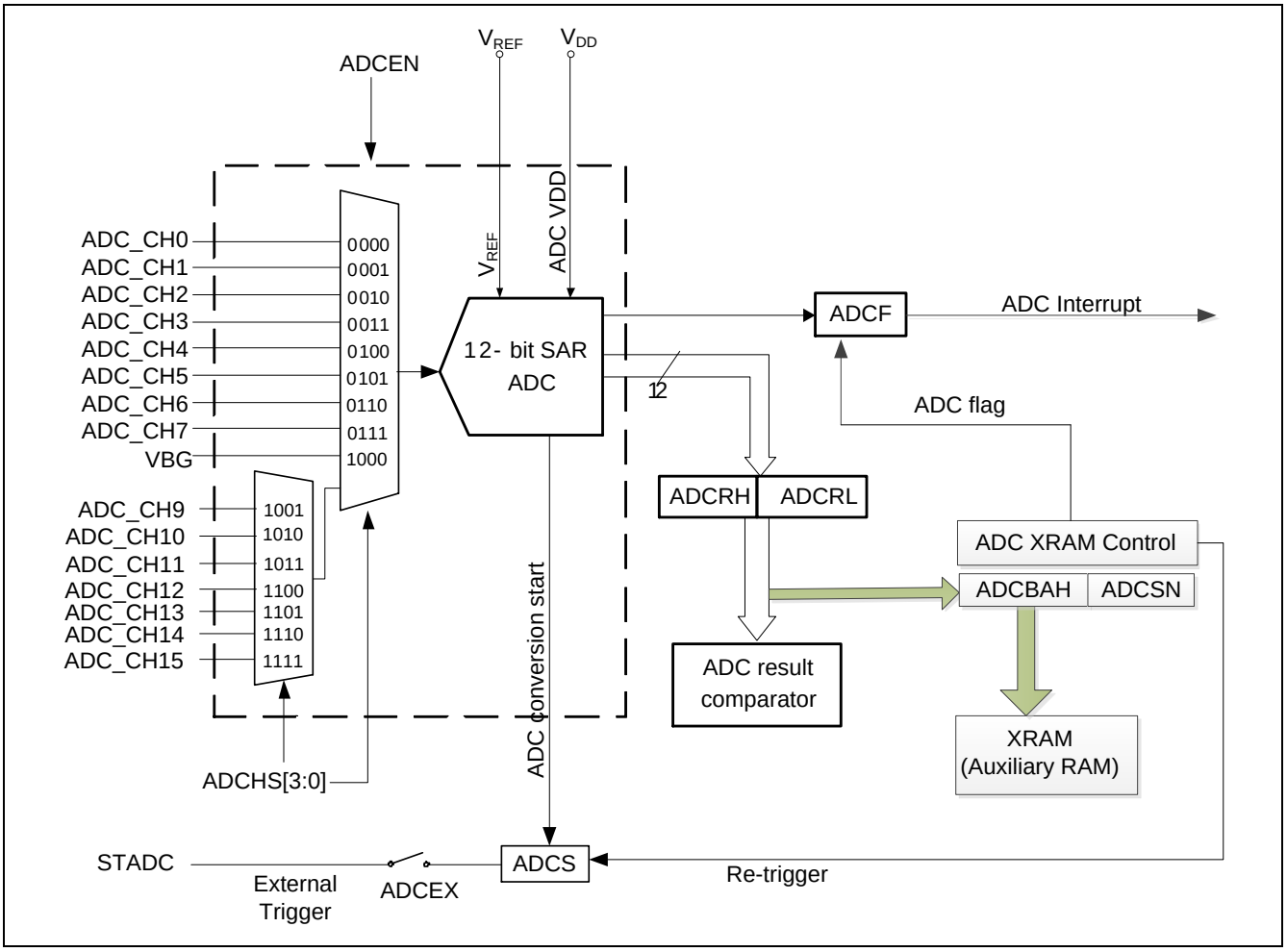

Figure 4-4 ADC Block Diagram for MS51 32KB Series

4.6.2.1 Register

Below is the list of new enhancements on MS51 32KB series:

- A new CONT (ADCCON3[4]) register has been added to set ADC into continues conversion mode.
- Two new ADCBAH and ADCBAL registers have been added to configure store address of conversion result.
- A new ADCCN register has been added to configure ADC conversion count.
- A new HIE(ADCCON3[5]) register has been added to enable ADC conversion half done interrupt.

Register	SFR Address	Reset Value
ADCCON3	86H, Page 2	0000_0000 b

7	6	5	4	3	2	1	0
-	-	HIE	CONT	ADCAQT1[2:0]			CKSWTF
-	-	R/W	R/W	R/W			R

Bit	Name	Description
[5]	HIE	**ADC Half Done Interrupt Enable** 0 = ADC interrupt is not set while half of A/D conversions are complete in continue mode 1 = ADC interrupt is set while half of A/D conversions are complete in continue mode
[4]	CONT	**ADC Continue Sampling select** 0 = ADC single sampling, ADC interrupt is set while an A/D conversion is completed 1 = ADC continue sampling. ADC interrupt is set while total A/D conversions are completed

Table 4-15 ADC Control Register 3 for MS51 32KB Series

Register	SFR Address	Reset Value
ADCCN	8EH, Page 2	0000_0000 b

7	6	5	4	3	2	1	0
ADCCN[7:0]-							
R/W							

Bit	Name	Description
[7:0]	ADCCN[7:0]	**ADC Current Sampling Number** The current sampling numbers for ADC continue sampling select. The current sampling number= ADCCN[7:0] + 1

Table 4-16 ADC Current Sampling Number for MS51 32KB Series

Register	SFR Address	Reset Value
ADCBAH	84H, Page 2	0000_0000 b

7	6	5	4	3	2	1	0
-				ADCBAH[3:0]			
-				R/W			

Bit	Name	Description
[3:0]	ADCBAH[3:0]	**ADC RAM base address (High byte)** The most significant 4 bits of RAM base address to store ADC continue sampling data. RAM base address ADCBA[11:0] = {ADCBAH[3:0], ADCBAL[7:0]}

Table 4-17 ADC RAM Base Address High Byte for MS51 32KB Series

Register	SFR Address	Reset Value
ADCBAL	85H, Page 2	0000_0000 b

7	6	5	4	3	2	1	0
ADCBAL[7:0]							
R/W							

Bit	Name	Description
[7:0]	ADCBAL[7:0]	**ADC RAM base address (Low byte)** The least significant 8 bits of RAM base address to store ADC continue sampling data. RAM base address ADCBA[11:0] = {ADCBAH[3:0], ADCBAL[7:0]}

Table 4-18 ADC RAM Base Address Low Byte for MS51 32KB Series

5 Migration Considerations Summary

5.1 Compatibility

- Hardware
  - The MS51 32KB series is fully pin-to-pin compatible with the MS51 16KB series on TSSOP20 and QFN20 packages and corresponding part number as shown in Table 2-4.
  - The MS51 32KB series includes a new feature, 4~24 MHz HXT selection.
- Software
  - Memory Map
    The MS51 32KB series APROM size is 32KB.
  - External Clock Source Selection
    The MS51 32KB series includes a new feature, 4~24 MHz HXT selection.
  - Interrupt Vector
    The MS51 32 KB series includes six new interrupt sources, PWM1/2/3 interrupt sources and SC0/1/2 interrupt sources.
  - PWM
    The MS51 32 KB series includes three new PWM modules, PWM1/2/3.
  - ISO 7816-3
    The MS51 32KB series includes a new feature, ISO 7816-3 interface controller.
  - ADC
    The MS51 32KB series includes a new feature, ADC continues conversion.
- Developing Tool
  1. The ICP Programming Tool should be updated to V3.00.6909 or later, as shown in Figure 5-1.
  2. If user needs to modify the source code, Nuvoton Nu-Link Keil should be updated to V3.02.6909 or later, as shown in Figure 5-2.

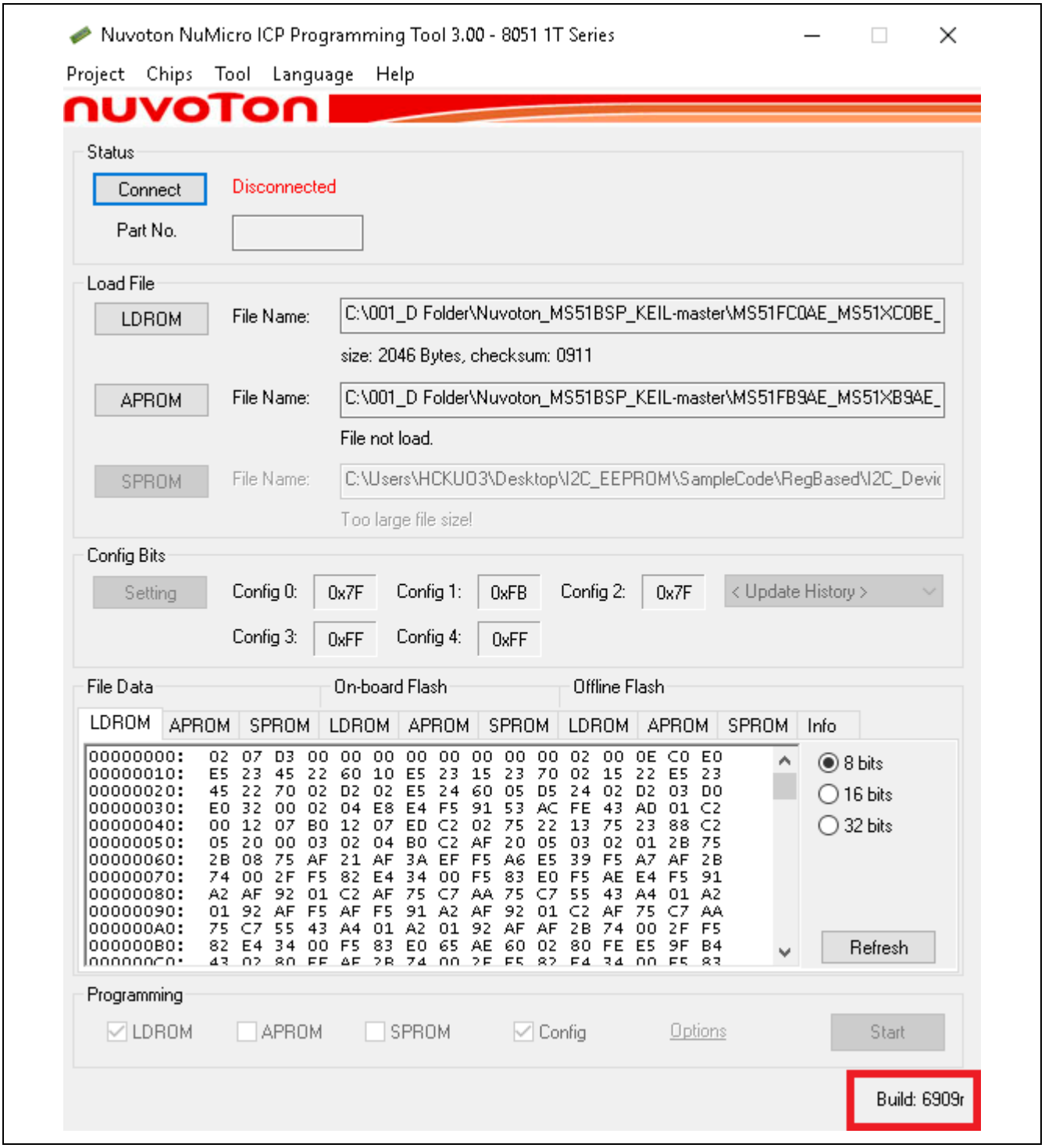

Figure 5-1 ICP Programming Tool Version

Figure 5-2 Nuvoton Nu-Link Keil Driver Version

6 Revision History

Date	Revision	Description
2020.11.30	1.00	1. Initially issued.

Important Notice

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