N76E003 Series to MS51 Series Migration and Performance Enhancement Guide

Migrating for 8-bit NuMicro® 8051 Family

Document Information

Abstract	This migration guide provides an overview of considerations for migrating from N76E003 series to MS51 16KB series, and includes migration considerations, the summary of the feature differences and the compatibility list of those enhanced features. Please refer to the summary of feature differences and the compatibility lists to determine the necessity of the code revision and make appropriate changes for the migration.
Apply to	NuMicro® MS51 16KB series.

For additional information or questions, please contact: Nuvoton Technology Corporation.

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1 Overview

The MS51 16KB series is a new enhanced version of N76E003 series. It is recommended to import the MS51 16KB series for new product design because the NuMicro® MS51 16KB series provides large portfolio of 8/16/32 KB. Since the MS51 16KB series is pin-to-pin compatible with the N76E003 series, the product can be easily upgraded by replacing the chip. Table 1-1 shows summary of migration considerations; Table 1-2 shows summary of enhanced features. The subsequent chapter details the migration considerations.

Item	Description
Package	● The MS51 16KB series is fully pin-to-pin compatible with the N76E003 series on TSSOP20 and QFN20 packages and corresponding part number as follows: MS51FB9AE ⇋ N76E003AT20 MS51XB9AE ⇋ N76E003AQ20 MS51XB9BE ⇋ N76E003BQ20
Peripheral	● APROM size adjusted from 18 KB to 16 KB ● ADCMP interrupt flag generation condition change. See section 3.3.1 for more details.
Tool	● ICP Programmer Tool V3.00.6909 or later ● Nu-Link Keil Driver V3.02.6909 or later ● Nu-Link IAR Driver V3.02.6909 or later

Table 1-1 Summary of Migration Considerations

Item	Description
Peripheral	● The RAM has increased from 256 + 768 Byte to 256 + 1K Byte ● Newly supported SPROM function ● Default HIRC frequency is 16 MHz, up to 24 MHz ● Please note that the HIRC will revert to 16 MHz after each power-up, and the user needs to change the HIRC frequency to 24 MH by set the HIRC24(RCTRIM1[4]). ● An enhanced ADC module for supporting clock divider as defined in ADCDIV(ADCCON1[5:4]), adjustable acquisition time as defined in ADCAQT(ADCCON2[3:1]) and slow speed selection as defined in SLOW(AUXR1[4]) ● An enhanced I^{2}C module for supporting I2C0_SDA hold time extend ● An enhanced I/O module for supporting high-current drive capability

Table 1-2 Overview of Enhanced Features in MS51 16KB Series

2 Peripheral Migration Guide

2.1 Peripheral Comparison Overview

The MS51 16KB series is a new member of enhanced version of 1T 8051. Table 2-1 to Table 2-3 show N76E003 series and MS51 16KB series peripheral comparison in pin compatible packages. The differences are highlighted in BLUE.

Part Number	Flash (KB)	SRAM (KB)	ISP ROM (KB)	I/O	Timer/	PWM	Connectivity				ADC(12-Bit)	Package
							ISO-7816	UART	SPI	I²C		
N76E003AT20	**18**	1	4	18	4	6	-	2	1	1	8-ch	TSSOP20
MS51FB9AE	16	1	4	18	4	6	-	2	1	1	8-ch	TSSOP20

Table 2-1 N76E003 Series and MS51 16KB Series Peripheral Comparison in TSSOP20

Part Number	Flash (KB)	SRAM (KB)	ISP ROM (KB)	I/O	Timer/	PWM	Connectivity				ADC(12-Bit)	Package
							ISO-7816	UART	SPI	I²C		
N76E003AQ20	**18**	1	4	18	4	6	-	2	1	1	8-ch	QFN20
MS51XB9AE	16	1	4	18	4	6	-	2	1	1	8-ch	QFN20

Table 2-2 N76E003 Series and MS51 16KB Series Peripheral Comparison in QFN20

Part Number	Flash (KB)	SRAM (KB)	ISP ROM (KB)	I/O	Timer/	PWM	Connectivity				ADC(12-Bit)	Package
							ISO-7816	UART	SPI	I²C		
N76E003BQ20	**18**	1	4	18	4	6	-	2	1	1	8-ch	QFN20
MS51XB9BE	16	1	4	18	4	6	-	2	1	1	8-ch	QFN20

Table 2-3 N76E003 Series and MS51 16KB Series Peripheral Comparison in QFN20

2.2 Peripheral Compatibility List

The differences and enhancements between the N76E003 series and MS51 16KB series are listed in Table 2-4.

Function	Compatibility		Description
	N76E003	MS51	
APROM	18 KB	16 KB	-
LDROM	Start from APROM address 3800H / 3C00H / 4000H / 4400H	Start from APROM address 3000H / 3400H / 3800H / 3C00H	-
SPROM	-	Start from FF80H	Newly supported SPROM function
HIRC	16 MHz	16 MHz (default) or 24 MHz (Need to reload trim value)	Newly supported 24 MHz HIRC selection
ADC	-	ADC clock divider	Newly supported ADC clock divider
	-	ADC clock slow mode select	Newly supported ADC clock slow mode selection
	-	ADC acquisition time select	Newly supported ADC acquisition time selection
ADCMP	-	-	ADCMP interrupt flag generation condition change
SPI	-	-	Full compatibility
I2C	-	I2C0_SDA pin hold time extend enable	Newly supported I2C0_SDA pin hold time extend 8 system clock
UART	-	-	Full compatibility
TIMER	-	-	Full compatibility
GPIO	-	-	Enhanced I/O drive capability

Table 2-4 N76E003 Series and MS51 16KB Series Comparison

Table 2-5 lists the pin compatible packages between N76E003 series and MS51 16KB series

N76E003 Series	MS51 Series	Package
N76E003AT20	MS51FB9AE	TSSOP 20
N76E003AS20	-	SOP 20
N76E003AQ20	MS51XB9AE	QFN 20*
Note:* QFN20 package with two kinds of different dimensions.		

Table 2-5 N76E003 Series and MS51 16KB Series Pin Compatible Packages

3 Software Migration Guide

3.1 Memory Organization

3.1.1 APROM

The APROM size between the N76E003 series and the MS51 16KB series is different. The APROM on the N76E003 series is 18 KB and the APROM on the MS51 16KB series is 16 KB.

3.1.2 SPROM

The MS51 16KB series supports a new feature, security protection memory (SPROM), which is used to secure application. SPROM includes 128 bytes at location address FF80H~FFFFH and does not support “whole chip erase command”.

3.2 Clock System

3.2.1 HIRC Switch from 16 MHz to 24 MHz

The HIRC in the N76E003 series supports maximum operating frequency of 16 MHz and the MS51 16KB series operating frequency default is 16 MHz that it compatible with N76E003 series. The MS51 16KB series operating frequency up to 24 MHz by set HIRC24 (RCTRIM1.4).

3.2.1.1 Register

The MS51 16KB series has a new HIRC24 bit (RCTRIM1[4]), which can be used to configure HIRC 24 MHz operating frequency. The register details are as follows:

- The new features are highlighted in BLUE and bits marked in “-“ are reserved.
- “All register pages” means that the register can access on page 0 and page 1.
- "Timed Access(TA)" means that the TA protected SFR have a timed write enable window. A writing permission window is opened for 4 clock cycles during this period that user may write to protected SFR. Otherwise, the write will be discarded. The suggested code for opening the timed access window is shown below.

```
TA = 0xAA; //First write 0xAA to the TA register and immediately followed by a write of 0x55 to TA register
TA = 0x55;
RCTRIM0 = 0x10; //A write is successful
```

Register	SFR Address	Reset Value
RCTRIM0	84H, All register pages, TA protected	0000_0000b

7	6	5	4	3	2	1	0
HIRCTRIM[8:1]							
R/W							

Table 3-1 High Speed Internal Oscillator Trim 0 for N76E003 Series

Register	SFR Address	Reset Value
RCTRIM1	85H, All register pages, TA protected	0000_0000b

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	HIRCTRIM.0
-	-	-	-	-	-	-	R/W

Table 3-2 High Speed Internal Oscillator Trim 1 for N76E003 Series

Register	SFR Address	Reset Value
RCTRIM0	84H, All register pages, TA protected	0000_0000b

7	6	5	4	3	2	1	0
HIRCTRIM[8:1]							
R/W							

Table 3-3 High Speed Internal Oscillator Trim 0 for MS51 16KB Series

Register	SFR Address	Reset Value
RCTRIM1	85H, All register page, TA protected	0000_0000b

7	6	5	4	3	2	1	0
-	-	-	**HIRC24**	-	-	-	HIRCTRIM.0
-	-	-	**R/W**	-	-	-	R/W

Bit	Name	Description
[4]	**HIRC24**	**HIRC 24 MHz Enable bit** 0 = 16 MHz 1 = 24 MHz

Table 3-4 High Speed Internal Oscillator Trim 1 for MS51 16KB Series

3.3 ADC

The main differences between the N76E003 series and the MS51 16KB series are:

- ADCMP interrupt flag generation condition change. See section 3.3.1 for more details.
- The MS51 16KB series includes a new feature, ADC clock divider. See section 3.3.2 for more details.
- The MS51 16KB series includes a new feature, ADC acquisition time selection. See section 3.3.3 for more details.
- The MS51 16KB series includes a new feature, ADC clock slow mode selection. See section 3.3.4 for more details.

3.3.1 ADCMP Interrupt Flag Generation Condition

The ADCMP interrupt flag generation condition between the N76E003 series and the MS51 16KB series is different.

The ADCMP interrupt flag generation condition on the N76E003 series is as follows:

- Set ADCMP enable bit, which is defined in ADCMPEN(ADCCON2[5])
- ADCF(ADCCON0[7]) is set when an A/D conversion is completed and ADCMPO (ADCCON2[4]) shows the compare result

The ADCMP interrupt flag generation condition on the MS51 16KB series is as follows:

- Set ADCMP enable bit, which is defined in ADCMPEN(ADCCON2[5]).
- Only when comparator value match the condition of ADC compare value defined, the interrupt flag will be set to 1.
    - The comparator value is stored in ADCMP[11:4](ADCMPH[7:0]) and ADCMP[3:0](ADCMPL[7:0]).
    - The new conversion result is stored in ADCR[11:4](ADCRH[7:0]) and ADCR[3:0](ADCRL[7:0]).
    - ADC comparator output polarity is stored in ADCMPOP(ADCCON2[6]).

3.3.1.1 Example Code

Note: Set ADCS(ADCCON0[6]) to trigger an A/D conversion after each A/D conversion is complete. The suggested code on the MS51 16KB series is shown below.

```
int main(void)
{
    while(!ADCF)
    {
        Set_ADCS;
    }
}
```

The code on MS51 16KB series shown below is not recommended. If the comparator value does not match with the conversion result, the code cannot set ADCS(ADCCON0[6]) to trigger an A/D conversion again.

```
int main(void)
{
    Set_ADCS;
    While(1)
    {
        while(ADCF == 1);
        Set_ADCS;
    }
}
```

3.3.1.2 Register

Please note that the ADCCON2 register should access SFR page 0 in the MS51 16KB series, but the N76E003 series is not restricted. The register details are as follows:

- The new features are highlighted in BLUE and bits marked in “-“ are reserved.
- “All register pages” means that the register can access on page 0 and page 1.

Register	SFR Address	Reset Value
ADCCON2	E2H, All register pages	0000_0000b

7	6	5	4	3	2	1	0
ADFBEN	ADCMPOP	**ADCMPEN**	ADCMPO	-	-	-	ADCDLY.8
R/W	R/W	**R/W**	R	-	-	-	R/W

Bit	Name	Description
[5]	**ADCMPEN**	**ADC result comparator enable** 0 = ADC result comparator Disabled 1 = ADC result comparator Enabled

Table 3-5 ADC Control Register 2 for N76E003 Series

Register	SFR Address	Reset Value
ADCCON2	E2H, **Page 0**	0000_0000b

7	6	5	4	3	2	1	0
ADFBEN	ADCMPOP	**ADCMPEN**	ADCMPO	ADCAQT[2:0]			ADCDLY.8
R/W	R/W	**R/W**	R	R/W			R/W

Bit	Name	Description
[5]	**ADCMPEN**	**ADC result comparator enable** ADC result comparator to trigger ADCF enable bit. Only when comparator value match the condition of ADC compare value defined ADCF will be set to 1. 0 = ADC result comparator trigger ADCF Disabled. 1 = ADC result comparator trigger ADCF Enabled. **Note**: After this bit is enabled and ADC start is triggered, the ADC keeps converting. The register ADCRH and ADCRL value will change based on the result of ADC setting and can also be read out from the register. This process only stops after ADCF is set to 1

Table 3-6 ADC Control Register 2 for MS51 16KB Series

3.3.2 ADC Clock Divider

The MS51 16KB series includes a new feature, ADC clock divider.

3.3.2.1 Register

The MS51 16KB series has a new ADCDIV bit (ADCCON1[5:4]), which can be used to configure ADC clock divider. Please note that the ADCCON1 register should access SFR page 0 in the MS51 16KB series, but the N76E003 series is not restricted.

The register details are as follows:

- The new features are highlighted in BLUE and bits marked in “-“ are reserved.
- “All register pages” means that the register can access on page 0 and page 1.

Register	SFR Address	Reset Value
ADCCON1	E1H, All register pages	0000_0000b

7	6	5	4	3	2	1	0
-	STADCPX	-	-	ETGTYP[1:0]		ADCEX	ADCEN
-	R/W	-	-	R/W		R/W	R/W

Table 3-7 ADC Control Register 1 for N76E003 Series

Register	SFR Address	Reset Value
ADCCON1	E1H, **Page 0**	0000_0000b

7	6	5	4	3	2	1	0
-	STADCPX	**ADCDIV[1:0]**		ETGTYP[1:0]		ADCEX	ADCEN
-	R/W	**R/W**		R/W		R/W	R/W

Bit	Name	Description
[5:4]	**ADCDIV[1:0]**	**ADC ADCAQT clock divider** This field define sampoing acquisition time clock divider value. 00 = FADCAQT = $F_{SYS}/1$ 01 = FADCAQT = $F_{SYS}/2$ 10 = FADCAQT = $F_{SYS}/4$ 11 = FADCAQT = $F_{SYS}/8$

Table 3-8 ADC Control Register 1 for MS51 16KB Series

3.3.3 ADC Acquisition Time Selection

The MS51 16KB series includes a new feature, ADC acquisition time selection.

3.3.3.1 Register

The MS51 16KB series has a new ADCAQT bit (ADCCON2[3:1]), which can be used to configure ADC acquisition time. Please note that the ADCCON2 register should access SFR page 0 in the MS51 16KB series, but the N76E003 series are not restricted.

The register details are as follows:

- The new features are highlighted in BLUE and bits marked in “-“ are reserved.
- “All register pages” means that the register can access on page 0 and page 1.

Register	SFR Address	Reset Value
ADCCON2	E2H, All register pages	0000_0000b

7	6	5	4	3	2	1	0
ADFBEN	ADCMPOP	ADCMPEN	ADCMPO	-	-	-	ADCDLY.8
R/W	R/W	R/W	R	-	-	-	R/W

Table 3-9 ADC Control Register 2 for N76E003 Series

Register	SFR Address	Reset Value
ADCCON2	E2H, **Page 0**	0000_0000b

7	6	5	4	3	2	1	0
ADFBEN	ADCMPOP	ADCMPEN	ADCMPO	**ADCAQT[2:0]**			ADCDLY.8
R/W	R/W	R/W	R	**R/W**			R/W

Bit	Name	Description
[3:1]	**ADCAQT**	**ADC acquisition time** This 3-bit field decides the acquisition time for ADC sampling, following by equation below: ADC acquisition time = $\frac{4 * ADCAQT + 6}{F_{ADC}}$. The default and minimum acquisition time is 6 ADC clock cycles. Note that this field should not be changed when ADC is in converting.

Table 3-10 ADC Control Register 2 for MS51 16KB Series

3.3.4 ADC Clock Slow Mode Selection

The MS51 16KB series includes a new feature, ADC clock slow mode selection. It supports 200 KSPS or 500 KSPS.

3.3.4.1 Register

The MS51 16KB series has a new SLOW bit (AUXR1[4])), which can be used to configure ADC sampling time. The register details are as follows:

- The new features are highlighted in BLUE and bits marked in "-" are reserved.
- "All register pages" means that the register can access on page 0 and page 1.

Register	SFR Address	Reset Value
AUXR1	A2H, All register pages	0000_0000b

7	6	5	4	3	2	1	0
SWRF	RSTPINF	HardF	-	GF2	UART0PX	0	DPS
R/W	R/W	R/W	-	R/W	R/W	R	R/W

Table 3-11 Auxiliary Register 1 for N76E003 Series

Register	SFR Address	Reset Value
AUXR1	A2H, All register pages	POR 0000_0000b, Software 1U00_0000b nRESET pin U100_0000b Others UUU0_0000b

7	6	5	4	3	2	1	0
SWRF	RSTPINF	HardF	**SLOW**	GF2	UART0PX	0	DPS
R/W	R/W	R/W	**R/W**	R/W	R/W	R	R/W

Bit	Name	Description
4	SLOW	**ADC Slow Speed Selection** This bit is used to select ADC low speed. 0 = High speed 500 KSPS 1 = Low speed 200 KSPS

Table 3-12 Auxiliary Register 1 for MS51 16KB Series

3.4 I^{2}C

3.4.1 Hold Time Extend on I2C0_SDA Pin

The I^{2}C in the MS51 16KB series includes a feature, hold time extend 8 system clock on I2C0_SDA pin.

3.4.1.1 Register

The MS51 16KB series has a new I bit (I2CON[7])), which can be used to enable hold time extend 8 system clock on I2C0_SDA pin. The register details are as follows:

- The new features are highlighted in BLUE and bits marked in "-" are reserved.
- "All register pages" means that the register can access on page 0 and page 1.
- "Bit addressable" means that the individual bits of these SFR may be directly accessed and modified.

Register	SFR Address	Reset Value
I2CON	C0H, All register pages, Bit addressable	0000_0000 b

7	6	5	4	3	2	1	0
-	I2CEN	STA	STO	SI	AA	-	I2CPX
-	R/W	R/W	R/W	R/W	R/W	-	R/W

Table 3-13 I^{2}C Control for N76E003 Series

Register	SFR Address	Reset Value
I2CON	C0H, all pages, Bit addressable	0000_0000 b

7	6	5	4	3	2	1	0
I	I2CEN	STA	STO	SI	AA	-	I2CPX
R/W	R/W	R/W	R/W	R/W	R/W	-	R/W

Bit	Name	Description
[7]	**I**	**I2C0 hold time extend enable** 0 = I2C DATA to I2C0_SCL hold time extend disabled 1 = I2C DATA to I2C0_SCL hold time extend enabled, extend 8 system clock

Table 3-14 I^{2}C Control for MS51 16KB Series

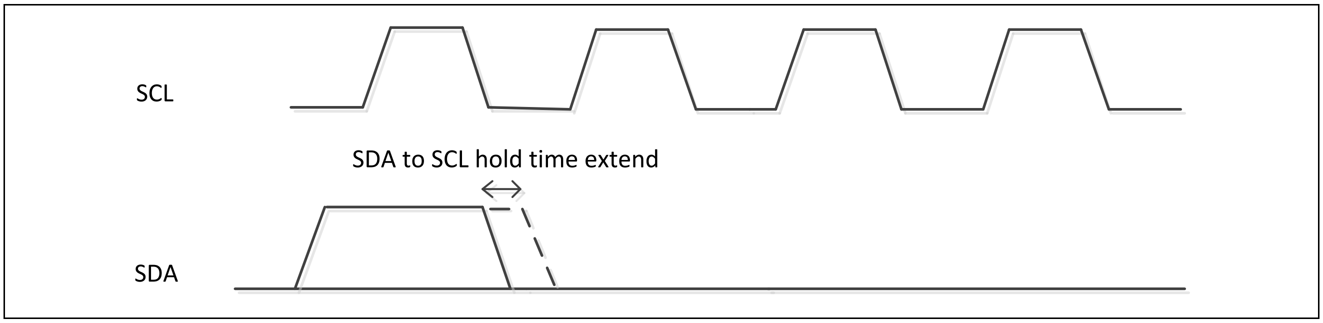


Figure 3.4-1 Hold Time Extend

3.5 GPIO

3.5.1 Enhanced I/O Drive Capability

The MS51 16KB series I/O module is an enhanced version of the N76E003 series. The I/O characteristics are shown in Figure 3.5-1 and Figure 3.5-2.

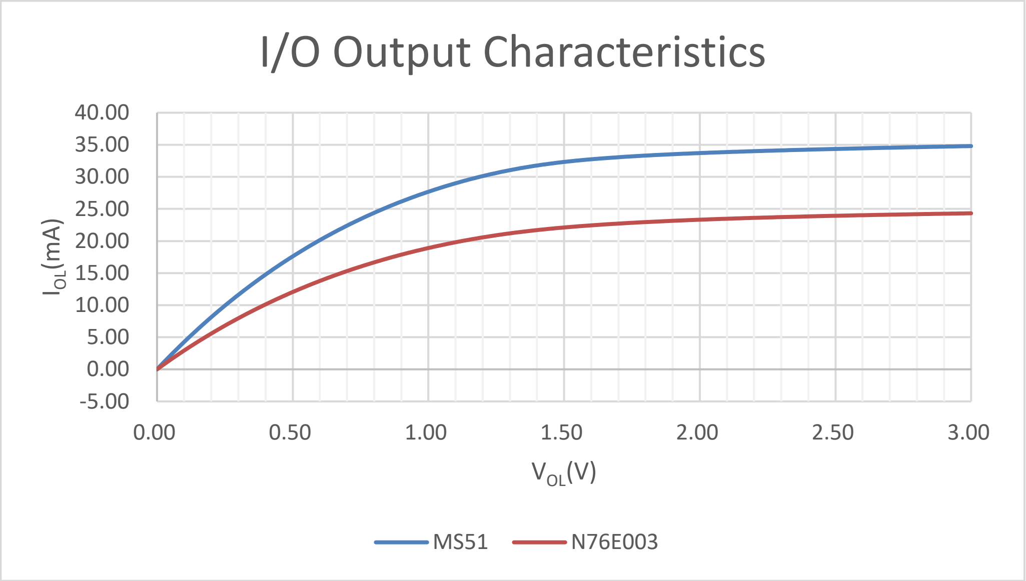


Figure 3.5-1 Output Sink Current (I_{OL}) VS. Output Voltage

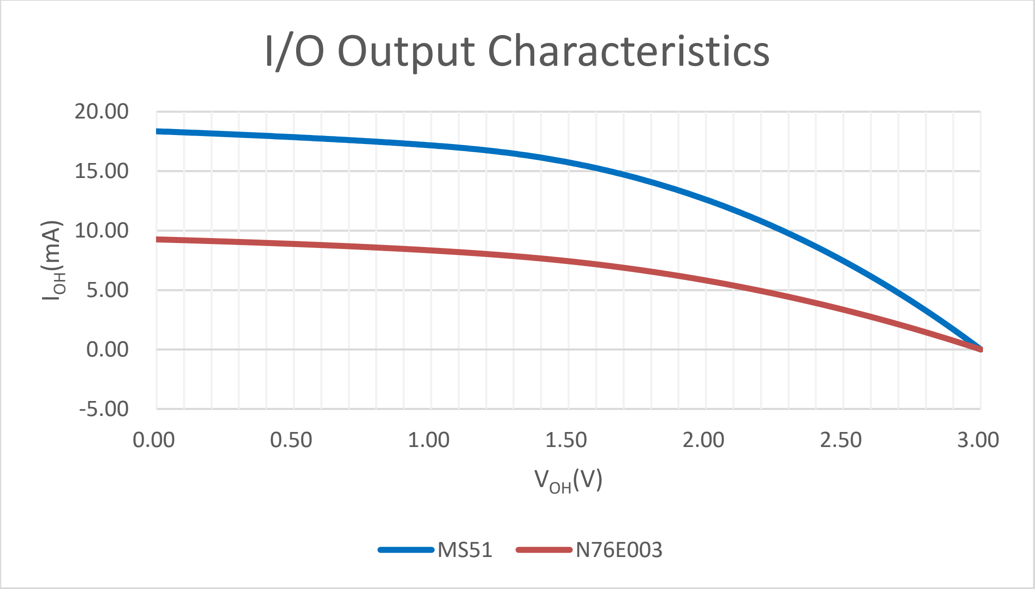


Figure 3.5-2 Output Source Current (I_{OH}) VS. Output Voltage

4 Migration Considerations Summary

4.1 Compatibility

- Hardware
  - ◆ The N76E003 series is fully pin-to-pin compatible with the MS51 16KB series on TSSOP20 and QFN20 packages and corresponding part number as shown in Table 2-5.
  - ◆ The MS51 16KB series supports enhanced I/O drive capability.
- Software
  - ◆ Memory Map

    The MS51 16KB series APROM size is 16 KB.

    The MS51 16KB series includes a new feature, SPROM.
  - ◆ HIRC

    The MS51 16KB series offers up to 24 MHz operation.
  - ◆ ADC

    The MS51 series includes three new features, ADC acquisition time selection, ADC clock divider and ADC speed selection.

    The MS51 16KB series document and source code can full compatibility with N76E003 series.

    The N76E003 series document and source code can partial compatibility with MS51 16KB series.
  - ◆ ADCMP

    The interrupt flag generation condition change.

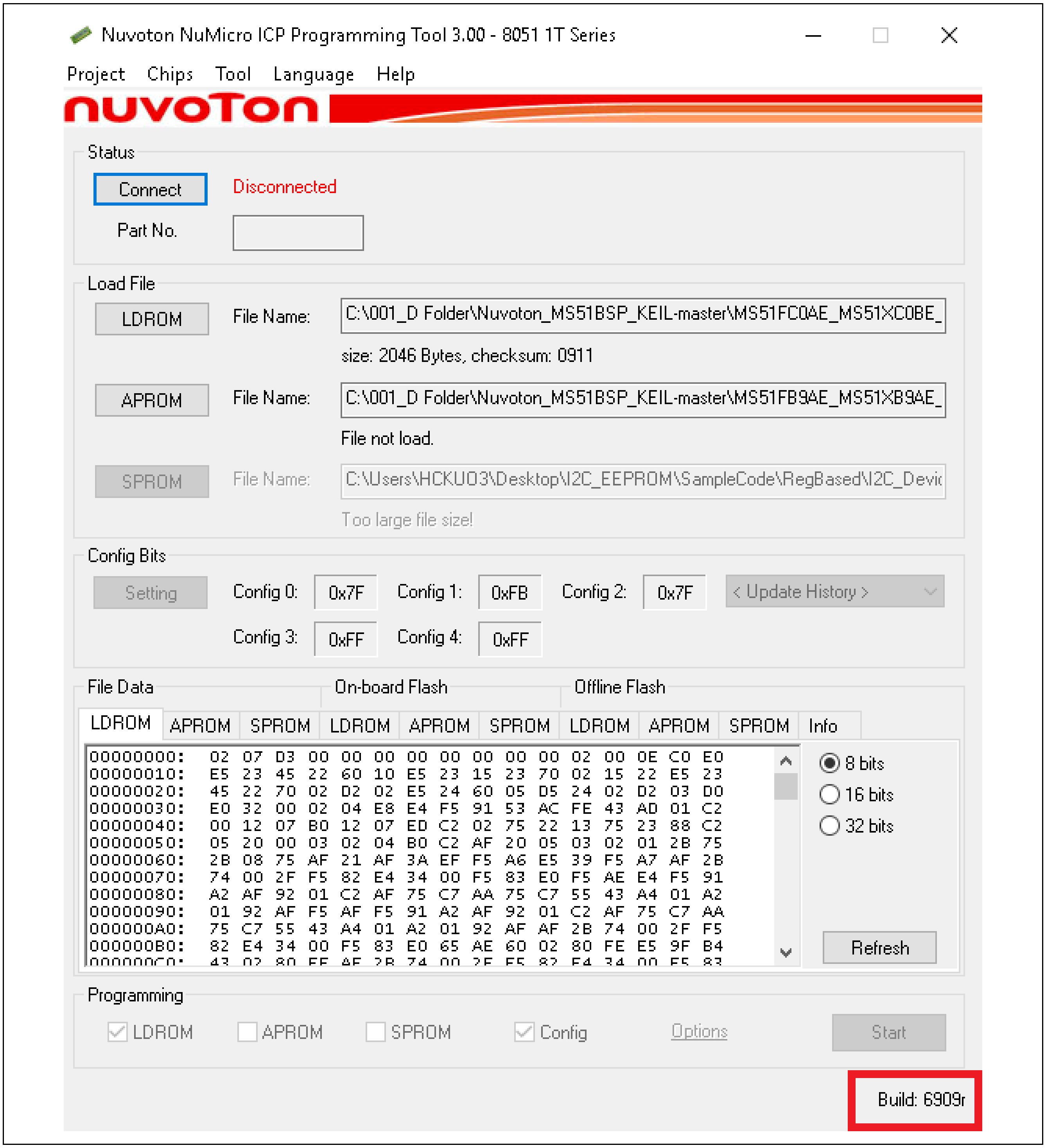
    The N76E003 series source code not compatibility with MS51 16KB series.

    In MS51 16KB series, only when comparator value match the condition of ADC compare value defined ADCF will be set to 1.
  - ◆ I^{2}C

    The MS51 16KB series includes a feature, hold time extend 8 system clock on SDA pin.
  - ◆ Hex and Bin files

    The MS51 16KB series Hex and Bin files can full compatibility with N76E003 series.
- Developing Tool
  1. The ICP Programming Tool should be updated to V3.00.6909 or later, as shown in Figure 4.1-1.

2. If user needs to modify the source code, Nuvoton Nu-Link Keil should be updated to V3.02.6909 or later, as shown in Figure 4.1-2.



Disconnected

Part No.:

File Name: C:\001_D Folder\Nuvoton_MS51BSP_KEIL-master\MS51FC0AE_MS51XC0BE_

size: 2046 Bytes, checksum: 0911

File Name: C:\001_D Folder\Nuvoton_MS51BSP_KEIL-master\MS51FB9AE_MS51XB9AE_

File not load.

File Name: C:\Users\HCKU03\Desktop\I2C_EEPROM\SampleCode\RegBased\I2C_Devic

Too large file size!

Config 0: 0x7F Config 1: 0xFB Config 2: 0x7F

Config 3: 0xFF Config 4: 0xFF

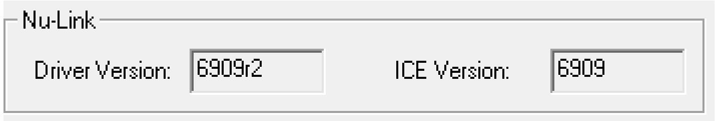
```
00000000:  02 07 D3 00 00 00 00 00 00 00 00 02 00 0E C0 E0
00000010:  E5 23 45 22 60 10 E5 23 15 23 70 02 15 22 E5 23
00000020:  45 22 70 02 D2 02 E5 24 60 05 D5 24 02 D2 03 D0
00000030:  E0 32 00 02 04 E8 E4 F5 91 53 AC FE 43 AD 01 C2
00000040:  00 12 07 B0 12 07 ED C2 02 75 22 13 75 23 88 C2
00000050:  05 20 00 03 02 04 B0 C2 AF 20 05 03 02 01 2B 75
00000060:  2B 08 75 AF 21 AF 3A EF F5 A6 E5 39 F5 A7 AF 2B
00000070:  74 00 2F F5 82 E4 34 00 F5 83 E0 F5 AE E4 F5 91
00000080:  A2 AF 92 01 C2 AF 75 C7 AA 75 C7 55 43 A4 01 A2
00000090:  01 92 AF F5 AF F5 91 A2 AF 92 01 C2 AF 75 C7 AA
000000A0:  75 C7 55 43 A4 01 A2 01 92 AF AF 2B 74 00 2F F5
000000B0:  82 E4 34 00 F5 83 E0 65 AE 60 02 80 FE E5 9F B4
```

● 8 bits
○ 16 bits
○ 32 bits

☑ LDROM ☐ APROM ☐ SPROM ☑ Config

Build: 6909r

Figure 4.1-1 ICP Programming Tool Version



Driver Version: 6909r2

ICE Version: 6909

Figure 4.1-2 Nuvoton Nu-Link Keil Driver Version

5 Revision History

Date	Revision	Description
2020.11.23	1.00	1. Initially issued.

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

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